Amendments to the Specification

Please replace the title with the following amended title:

SEMICONDUCTOR MEMORY WITH SELF FUSE PROGRAMMING

Please replace the paragraph beginning at page 2, line 3, with the following rewritten paragraph:

As a fuse array for storing a save address, there is generally known a laser fuse for ~~breading~~ breaking a fuse by using a laser beam. Because a program of the save address for the laser fuse uses a laser beam, such programming can be carried out only in a wafer state, and cannot be carried out after an assembling process.

Please replace the paragraph beginning at page 3, line 16, with the following rewritten paragraph:

The data A0 to A4 are provided to a decoder circuit DCi. The decoder circuit DCi decodes the data A0 to A4, and generates fuse program data D0 to D19. The fuse program data ~~0~~ D0 to D19 determine a fuse targeted for fuse blowing.

Please replace the paragraph beginning at page 33, line 9, with the following rewritten paragraph:

TMCOMP is provided as a control signal for determining whether or not entry is made in the test mode (pseudo read cycle). For example, a period of TMCOMP = "H", the test mode is executed. The control signal ~~RMCOMP~~ TMCOMP is provided to the input circuit 14, the pseudo read control circuits 15 and 16, and the output circuit 17, and the states of these circuits in the test mode is determined.

Please replace the paragraph beginning at page 34, line 20, with the following rewritten paragraph:

For example, when the normal write mode is established, the control signal ~~RMCOMP~~ TMCOMP and the control signal bWRITE are set to "L", and thus, an

output signal bWTIN of the NAND gate circuit NAND1 is set to "H". As a result, the program data provided to the external input/output terminal 12 is outputted as program data WD from the input circuit 14.

Please replace the paragraph beginning at page 42, line 9, with the following rewritten paragraph:

In a read operation during the test mode (pseudo read cycle), since the control signal ~~RMCOMP~~ TMCOMP is set to "H", the output data compR is in the same phase as the input data (read data) RD. The output data RDD always maintains "L".

Please replace the paragraph beginning at page 50, line 23, with the following rewritten paragraph:

The latch circuit LA0 is composed of: a master data latch circuit MASTL; save address (save solution) latch circuits A0L to A3L; and a ~~band~~ bank address data latch circuit BanL.